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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/604,206 | 07/01/2003 | Andres Bryant | BUR920030003US1 | 1205 |

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| EXAMINER | |
|---|---|
| KANG, DONGHEE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/604,206 | BRYANT ET AL. | |
| | Examiner | Art Unit | |
| | Donghee Kang | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9 and 34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,4,7 and 8* is/are allowed.

6)☒ Claim(s) *1,2,5,6,9 and 34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Remarks*

1. Applicant's amendment and Response have been entered and made of record. Claims 10-33 are cancelled and new claims 34-42 are added. Thus claims **1-9 & 34-42** are pending in this instant application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-2, 6, 9, & 36** are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (US 6,770,516).

Re claim **1**, Wu et al. teach an integrated circuit structure utilizing fin-type field effect transistor (FinFETs) comprising (Fig.9-10):

A first FinFET(NMOS, 5) having a first fin; a second FinFET (PMOS, 6) having a second fin running parallel to said first fin, wherein said first FinFET comprising a separate transistor from said second FinFET (Col.4, lines 60-67); and an insulating fin (9) positioned between said first fin and said second fin.

Re claim **2**, WU et al. teach the integrated circuit structure further comprising a common gate (8) formed over channel regions of said first FinFET and said second FInFET.

Re claim **6**, Wu et al. teach an integrated circuit structure utilizing complementary fin-type field effect transistor (FinFETs) comprising (Fig.9-10):

A first FinFET(NMOS, 5) having a first fin; a second FinFET (PMOS, 6) having a second fin running parallel to said first fin, wherein said first FinFET comprising a separate transistor from said second FinFET (Col.4, lines 60-67); an insulating fin (9) positioned between said first fin and said second fin; and a common gate (8) formed over channel regions of said first-type of FinFET and said second-type of FinFET.

Re claim **9**, Wu et al. teach said first fin and said second fin have approximately the same width.

Re claim **36**, Wu et al. teach said first-type of FinFET is complementary to said second-type of FinFET.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **34-35 & 37-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 6,770,516) in view of Lin et al. (US 6,800,910).

Re claims **34-35 & 37**, Wu et al. teach an integrated circuit structure utilizing fin-type field effect transistor (FinFETs) comprising (Fig.9-10):

A first FinFET(NMOS, 5) having a first fin; a second FinFET (PMOS, 6) having a second fin running parallel to said first fin, wherein said first FinFET comprising a separate transistor from said second FinFET (Col.4, lines 60-67); an insulating fin (9) positioned between said first fin and said second fin. source and drain contacts of said first FinFET are electrically separated from source and drain contacts of said second FinFET.

Wu et al. do not explicitly show the source and drain contacts of said first FinFET are electrically separated from source and drain contacts of said second FinFET. However, Lin et al. teach in Fig.8 the complementary FinFETs (90 & 92) including source/drain contacts for NFET and PFET which are separated electrically from each other. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form source/drain contact for NFET and PFET electrically separately from each other in order to obtain a desire operation for CMOS FET.

Re claim **38**, Wu et al. teach said first fin and said second fin have approximately the same width.

Re claim **39**, Wu et al. teach said first-type of FinFET is complementary to said second-type of FinFET.

Re claim **40**, WU et al. teach the integrated circuit structure further comprising a common gate (8) formed over channel regions of said first FinFET and said second FInFET.

Re claims 34 & 35, WU et al. teach the integrated circuit structure further comprising source and drain contacts connected to ends of said first fin and said second fin, wherein source and drain contacts (40) of said first FinFET are electrically separated from source and drain contacts (30) of said second FinFET.

6. Claims **41-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 6,770,516) in view of Lin et al. (US 6,800,910) as applied to claim 37 above, and further in view of Yuzurihara et al. (US 5,218,232).

Neither Wu nor Lin teaches the gate includes first impurity doping region and second impurity doping region, wherein said first impurity doping region and said second impurity doping region provide gate with different work function related between NFET and PFET. However, Yuzurihara et al. teach in Figs.7-8 the gate includes first impurity doping region (10) and second impurity doping region (9), wherein said first impurity doping region and said second impurity doping region provide gate with different work function related between NFET and PFET to match the threshold voltages. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form gate electrode having first impurity doping region and said second impurity doping region provide gate with different work function related between NFET and PFET in order to satisfy matching in a complementary circuit.

***Allowable Subject Matter***

7. Claims **3-4 & 7-8** are allowed.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk